TU Clausthal

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„Reactive Synthesis of a AXI Bus Client on a FPGA“

In the evolving landscape of digital technology, System-On-Chip (SoC) play a crucial role in applications ranging from smartphones and IoT devices to automotive control systems.The Communication within SoC is often facilitated by bus systems like Advanced eXtensible Interface Advanced (AXI) Lite protocol being a widely adopted standard for control and configuration tasks. However, implementing a correct and reliable AXI-Lite slave component can be challenging due to the protocol's complexity and the risk of design errors in manual implementations.

This thesis explores the use of reactive synthesis as a formal approach to automatically generate correct by construction an AXI bus client. Reactive synthesis derives systemlogic directly from high-level specifications, reducing the likelihood of implementation errors. Unlike traditional manual coding approaches, this method ensures compliance with protocol requirements while providing a flexible Framework for rapid adaptation to different AXI-based clients or other application. The synthesis process is carried out using modern tools Bounded Synthesis ,which generates Verilog code based on LTL Specifications].To validate the synthesized design, the implementation is deployed on a StemLab 125-10 Field Gate Programmable Array (FPGA) board featuring a Xilinx Zynq 7010 FPGA . The correctness of the generated hardware is verified using Vivado, confirming its functionality in a real world FPGA environment. By demonstrating how minor modifications to the high-level specification can yield different AXI-Lite-compliant clients, this work highlights the adaptability and efficiency of reactive synthesis in SoC design.This thesis contributes to the advancement of automated hardware design methodologies by showcasing the feasibility of using reactive synthesis for bus protocol implementations. The approach not only mitigates the risks associated with manual development but also establishes a scalable and reusable framework for generating verified AXI-Lite clients, thereby enhancing reliability in SoC architectures.

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